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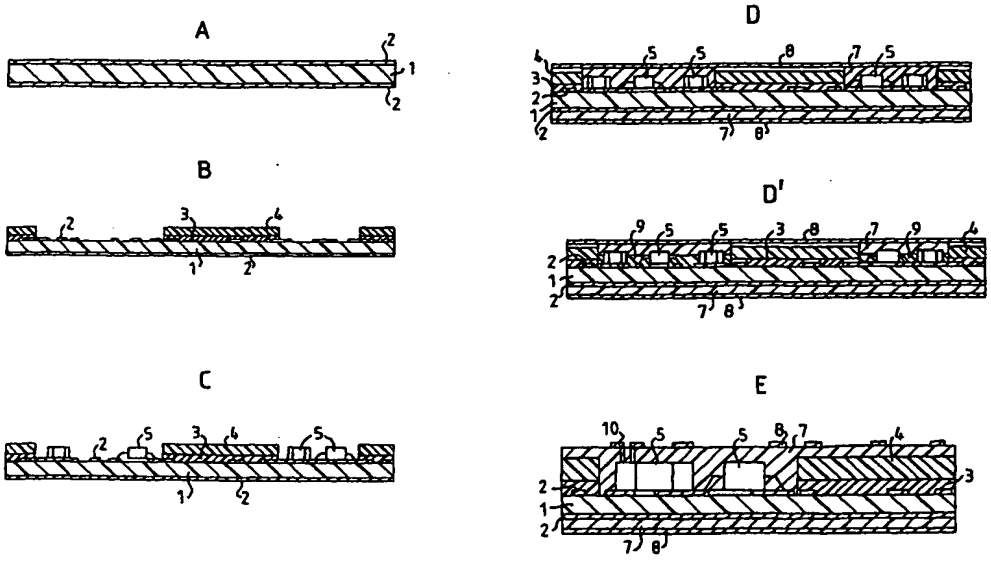

(57) Abstract

A compact printed board assembly has a patterned copper-coated substrate (1) with electronic components (5, 12) mounted thereon. Depending on the height of the components, either SBU lacquer (11) or non-flow prepreg (3) and laminate (4) surround the electronic components. This subassembly is then sandwiched between two RC (resin coated) copper foils (8) with the resin (7) facing the components (5, 12) and burying them, thereby providing a new etchable copper surface which can be connected by means of microvias (10) to the embedded components (5, 12).

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Printed board assembly and method of its manufacture

TECHNICAL FIELD OF THE INVENTION

The present invention relates to a printed board assembly, comprising a copper coated substrate with electronic components mounted thereon. The substrate with components are sandwiched between resin coated foils thus embedding the components. The invention also relates to a method of manufacturing such a printed board assembly.

DESCRIPTION OF RELATED ART

EP 0 813 355 (A2) to International Business Machines Inc. relates to a printed circuit board construction with stacked capacitive planes. The entire stack is then covered with epoxy glass to which copper foil is then applied. EP 0 813 355 (A2) does not provide for embedding anything other than flat capacitive planes, having an etched outer surface to which the epoxy adheres and bonds the copper foil.

Similarly, DE-A 196 34 016 (A1) to Taiyo Ink Mfg. Co. Ltd. describes coating a printed circuit board having circuit patterns etched therein with resin and laying a similar etched copper layer thereon which is in turn coated with resin. This reference, as that described above, does not describe anything other than the embedding of flat etched copper sheets.

SUMMARY OF THE INVENTION

A printed board assembly is provided comprising a substrate coated with an electrically conducting material, such as etched copper, electrical components being mounted on said substrate, said substrate with components being covered on both sides with resin coated conducting foil, the resin of said resin coated foil facing the substrate and burying said components, said foil being etched with a circuit pattern, a non-conducting material being disposed in the areas between said electrical components.

The present invention enables more components to be packed more compactly within and on the carrier, thereby making it possible to improve the electrical performance and to integrate the electrical shielding in the carrier. The mechanical stability and strength of the entire assembly is also improved.

According to one embodiment of the printed board assembly according to the present invention, said components are chip resistors and that said carrier is coated between said chip resistors with a sequential built-up (SBU) lacquer. The lacquer is applied in the areas between the chip resistors sequentially until it reaches the level of the top surfaces of the chip resistors, whereupon the resin coated foil is easily applied to the essentially flat surface. This is a very simple and low cost method of integrating chip resistors into the carrier.

According to another embodiment of the printed board assembly according to the present invention said carrier is covered in the areas between said components with a preimpregnated non-conducting resin mat or prepreg covered with a laminate, both provided with holes for said components. This enables the principle of the invention to be applied when higher components than chip resistors are mounted on the substrate. There is either sufficient resin to fill out any remaining space between these higher electronic components, or alternatively, these small remaining spaces can be coated with SBU lacquer before the resin coated foil is applied thereon.

A method is also provided for manufacturing such a printed board assembly, comprising the steps of: mounting electronic components on a substrate coated with patterned copper; covering only the areas of the copper coated substrate between the mounted components with a non-conducting material approximately up to the level of the mounted components, sandwiching the substrate, components and non-conducting material between two sheets of resin coated conducting foil, the resin on said foils facing the substrate and burying said components, and etching circuit patterns in the exposed copper surfaces of the resin coated conducting foils. This is a

very economical way of achieving vertical packing of many components in a way which is advantageous structurally and electrically.

BRIEF DESCRIPTION OF THE DRAWINGS

Figs. 1(a-e) show the sequence of steps in manufacturing a printed board assembly of the present invention in accordance with one embodiment of the invention.
Figs. 2(a-e) show the sequence of steps in manufacturing a printed board assembly of the present invention in accordance with another embodiment of the invention.

DETAILED DESCRIPTION OF EMBODIMENTS

Fig. 1 shows the method of the present invention in a first embodiment starting at step 1(a) with a standard copper coated 2 substrate 1. In step 1(b), at least one of the copper coatings 2 on the substrate is etched in the known manner to provide a circuit pattern and then a non-conducting prepreg 3 and laminate 4, which have been machined to create holes for the areas where the electronic components are to be mounted, are pressed together with the substrate 1. The prepreg is a resin impregnated mat of "non-flow" type.

The electronic components 5, which in this case can be integrated circuit components etc., are then mounted in the openings in the prepreg 3 and laminate 4. This is shown in step 1(c).

The subassembly comprising the copper coated substrate 1, the prepreg 3 and the laminate 4 are then sandwiched between two resin coated copper foils 8 so that the resin 7 faces inwards. The result is shown in Fig. 1(d).

It may be the case that the resin 7 does not fill the spaces under and around the electronic components 5. In that case a lacquer, which may be an SBU (sequentially built-up) lacquer 9 is applied over the electronic components. This variant is shown in Fig. 1(d').

At least one of the foils 8 is then etched to form another printed circuit layer and microvia holes 10 are made connecting the foil 8 layer to the electronic components. This assembly is shown in Fig. 1(e). It is a multi-layer assembly providing exceptional structural stability and compact arrangement of many circuits. Heat can also be dissipated through the via holes.

Another embodiment of the invention is shown in Figs. 2(a-e) which show it applied to a printed board assembly which embeds only chip resistors under RC foil. The steps are essentially those described in relation to the embodiments shown in Figs. 1(a-e) and the corresponding components have been given the same reference numerals as in Figs. 1(a-e), with the exception that the non-conducting material disposed in the areas between the electrical components is only SBU lacquer. The prepreg and the laminate used in the embodiments shown in Figs. 1(a-e) are not necessary since chip resistors are rather thin.

Fig 2 (a) shows a standard copper-coated substrate 1. A photosensitive dielectric material 11 is painted onto the copper 2 on one side, and openings are made therein, (Fig. 2(b), into which chip resistors 12 are mounted (Fig. 2 (c).

This subassembly is then sandwiched, as in the example above, between two resin coated copper foils 8 so that the resin 7 faces inwards. The result is shown in Fig. 2(d).

As in the example above, at least one of the foils 8 is then etched to form a printed circuit layer and microvia holes 10 are made connecting the chip resistors 12 with the foil layer 8. This assembly is shown in Fig. 2(e), which allows the chip resistors and other passive components to be embedded leaving space exposed on the upper layer for more active components. The chip resistors 12 may also be contacted by soldering to the patterned copper coating 2 on the substrate 1. This method provides great flexibility as regards contacting the components.

It is of course also possible to repeat the process and build up even more layers on top of the foil layer 8.

CLAIMS

1. Printed board assembly, comprising:

(a) a substrate (1) coated with an electrically conducting material, such as patterned copper (2),

(b) electrical components (5; 12) mounted on some areas of said substrate,

(c) a non-conducting material (3,4;11) disposed in areas between said electrical components (5;12),

(d) resin coated conducting foil (8) covering both sides of said substrate including components(5;12) and non-conducting material (3,4;11),

the resin (8) of said resin coated foil facing the substrate and burying said components, said foil (8) being etched with a circuit pattern.

2. Printed board assembly according to Claim 1, wherein said components are chip resistors (12) and that said carrier is coated between said chip resistors with a sequential built-up (SBU) lacquer (11).

3. Printed board assembly according to Claim 1, wherein said carrier is covered in the areas between said components with a preimpregnated non-conducting resin mat or prepreg (3) covered with a laminate (4), both provided with holes for said components (5).

4. Method of manufacturing a printed board assembly, comprising the following steps:

(a) providing a substrate (1) coated with copper (2),

(b) making a circuit pattern in said copper and covering only the areas of the copper coated substrate lying between areas for mounting electronic components with a non-conducting material (3,4; 11) approximately up to the level of the components when mounted,

(c) mounting electronic components (5) on said substrate (1) coated with copper (2),

(d) sandwiching the substrate (1), components (5) and non-conducting material between two sheets of resin coated conducting foil (8), the resin (7) on said foils (8) facing the substrate and burying said components (5),

(e) etching circuit patterns in the exposed copper surfaces of the resin coated conducting foils (8),

(f) establishing electrical connections between at least one of said conducting foils (8) and said electronic components (5).

5. Method according to Claim 4, wherein said components (5) are chip resistors and the areas of the copper coated substrate (1) between the chip resistors (12) are covered a sequentially built up (SBU) lacquer (11).

6. Method according to Claim 4, wherein said components are electronic components (5) of greater thickness than chip resistors, and the areas between the electronic components are covered with prepreg (3) and a laminate (4) which have been provided with holes corresponding to the positions of said electronic components.

7. Method according to Claim 4, wherein the electrical connections are microvias (10).

8. Method according to Claim 6, wherein the electronic components are also covered with a coating of lacquer (9) between steps (c) and (d).

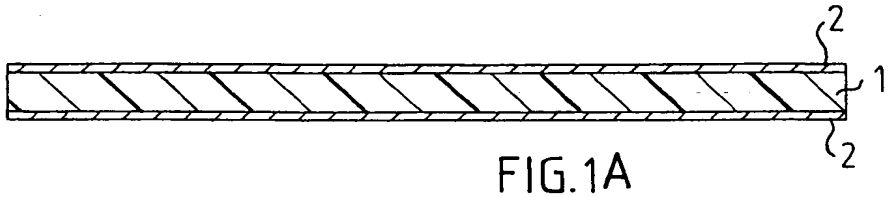

FIG. 1A

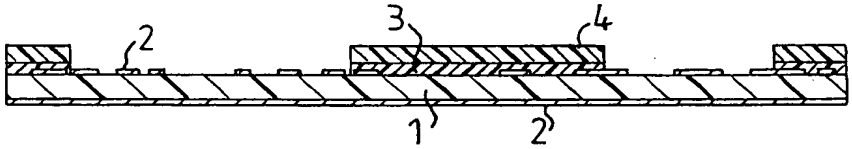

FIG. 1B

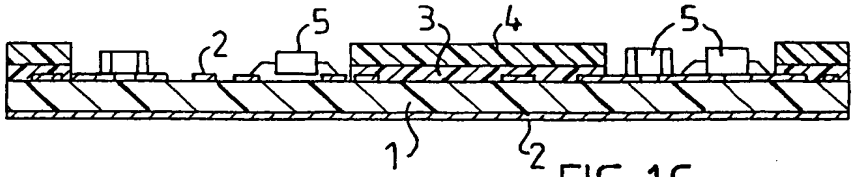

FIG. 1C

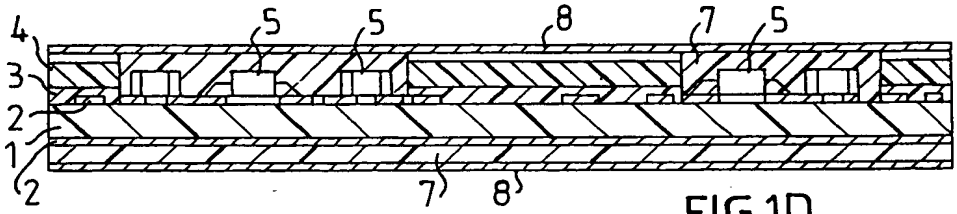

FIG.1D

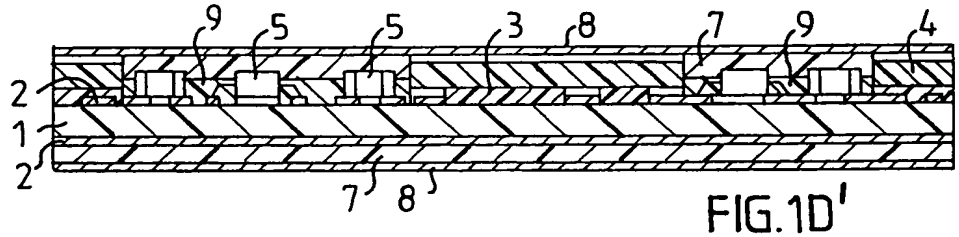

FIG.1D'

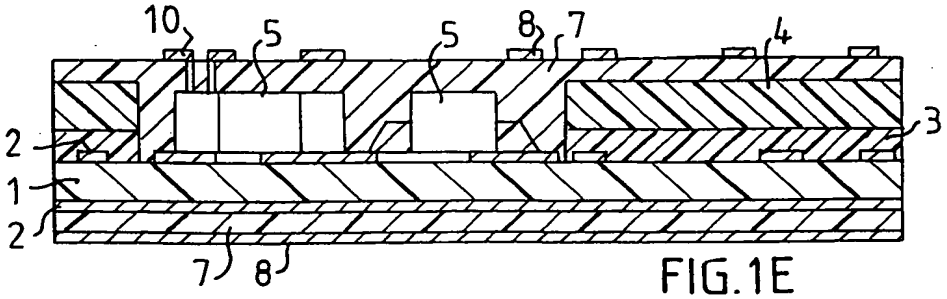

FIG.1E

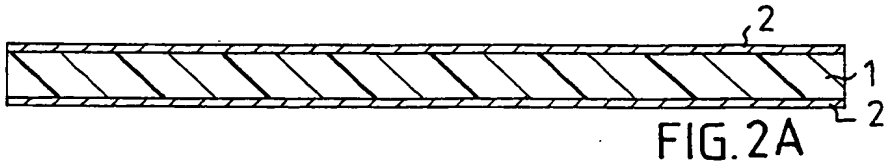

FIG. 2A

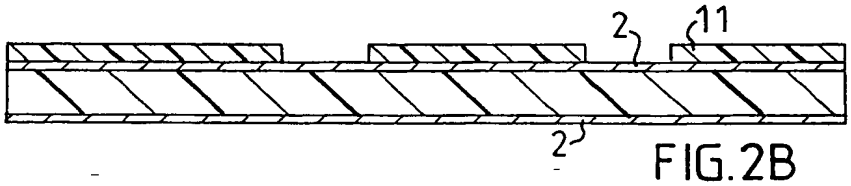

FIG. 2B

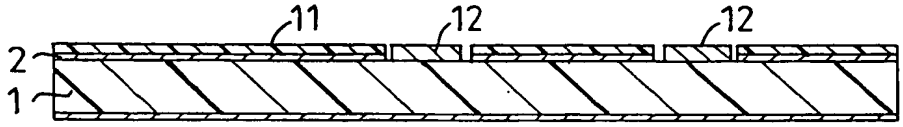

FIG. 2C

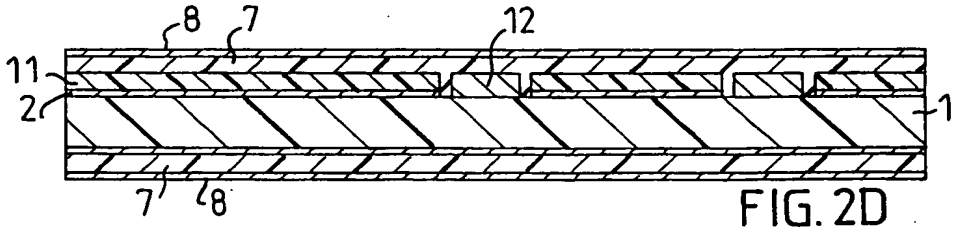

FIG. 2D

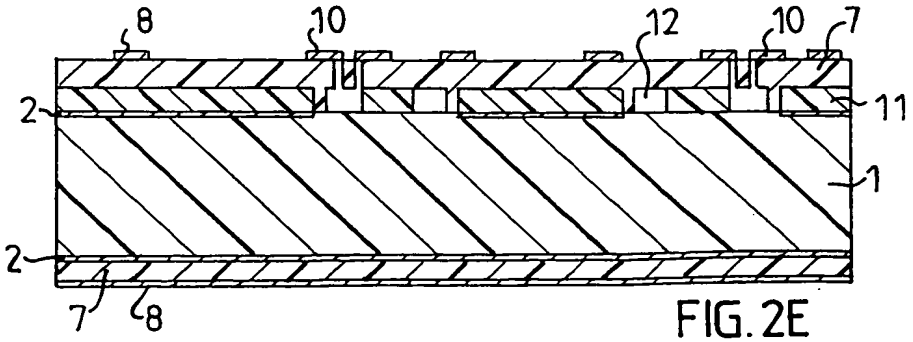

FIG. 2E